INSTRUCTION DATA

RFL Industries, Inc. • A Dowty Group Company

Model 66 CMDGEN
COMMAND GENERATOR CARD

DESCRIPTION

Model 66 CMDGEN is one of the RFL 66 TDMS Series of plug-in logic cards. It interfaces operator-actuated voltages or contacts and other cards associated with Mode and Command logic within a Master Station. This card is intended for use in systems which transmit a single message, only once, per command as opposed to continuously scanning systems.

There are provisions for eight commands: Point Select, Point Cancel, Execute A, Execute B, Execute C, Execute D, Execute E, and Execute F. This card will work in Select/Operate, Select/Check/Operate, Direct Operate and Proportional Control systems. Also included is an aperture timer, programmable from 0 to 40 seconds suitable to lock out commands, send Point Cancel messages and clear local point memory.

Other functions incorporated on the card are a clock to time other system modules and a power turn-on pulse for system initialization. The internal circuits will operate from Form A or Form B contacts and are insensitive to normal bounce.

A complementary Command Decoder Card Model 66 CMDEC is available for use in Remote Stations to receive the commands and provide the respective output pulses.

SPECIFICATIONS

Ambient Temperature: −30 to +70°C.

Power: 11 to 13 Vdc @ 10 mA.

Size: One standard one-half-inch module space in an RFL Model 68 Chassis.

PROGRAMMING AND CONNECTION

This module contains CMOS logic circuits and special handling precautions should be observed. Refer to "CMOS Handling Precautions", RFL Document 12175.

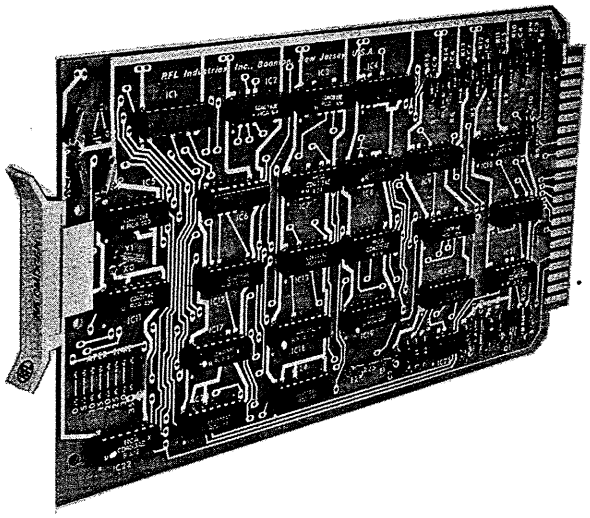

Figure 1. Model 66 CMDGEN Command Generator.

All unused input terminals or unused inputs to integrated circuits must be returned to +V or common. Jumpers used for programming, and their locations, are shown on Figure 2.

Input voltages or contacts are connected to Terminals 3 through 9 and 11. Each of these inputs has a 47KΩ resistor which will become a pull-down if the VO Jumper is installed or a pull-up if the V1 Jumper is used. If any of the inputs are driven from the A ACTIVE or B ACTIVE outputs of a 66 SLTC, then the VO Jumper must be installed.

INPUT LINES

V JUMPER

When any of those eight inputs goes to a logic 1, the appropriate command message will be sent. If two or more inputs are activated simultaneously, the command with the highest priority will be sent. The priorities from high to low are PT CANCEL, PT SELECT, and EXECUTE A through F.

When any input goes high and stays high, and if the W1 Jumper is installed, one and only one message will be sent no matter how long the input is high. However, repeated action can be obtained for the EXECUTE C and EXECUTE D commands by installing Jumper WO. Repeated action means that as long as the operator has his finger on the button, the appropriate command will be repetitively sent. With the WO Jumper installed the CIP signal from the 66 ENC/L will be

W JUMPER

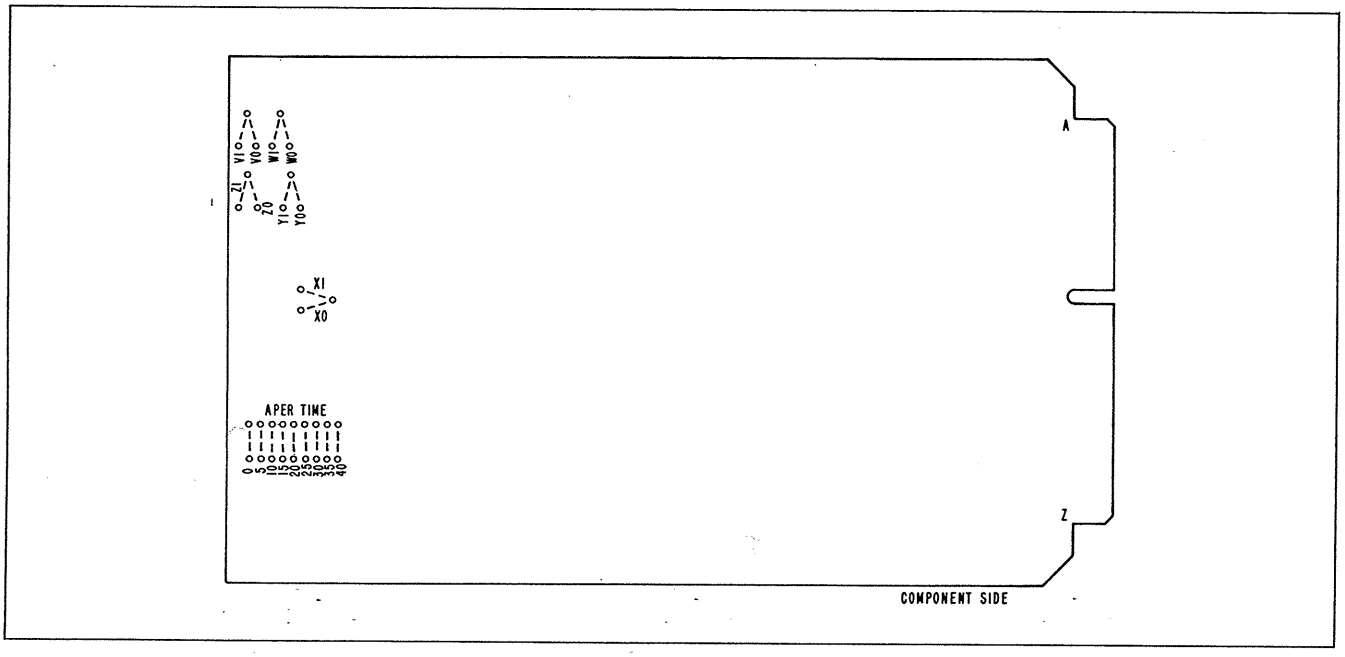

Figure 2. Card outline, showing location of jumpers used for programming.

gated with the input line to make the circuitry look like the operator were rapidly depressing and releasing the button. Repeated control is only available for the EXECUTE C and D commands.

The EXECUTE A, B, C, and D commands may be gated with the $\overline{\text{VERIFY}}$ signal and the aperture timer. If it is desired to lock out or prevent those four commands from being sent until $\overline{\text{VERIFY}}$ = 0, as in check-back systems, then Terminal R is wired to a suitable signal source such as that from a 66 COMP card. If that requirement does not exist, as in Direct Operate systems, Terminal R must be tied to common.

$\overline{\text{VERIFY}}$

The Z Jumper is used to gate the EXECUTE A, B, C, and D commands with the aperture timer. When the Z0 Jumper is installed, those four commands cannot be sent until the aperture timer has been restarted by a PT SELECT command. If aperture controlled lock-out is not used, then the Z1 Jumper should be installed. Z1 is used for Direct Operate systems.

Z JUMPERS

PT CANCEL, PT SELECT, EXECUTE E and EXECUTE F commands do not have any lock-out or verify gating and may be used at any time. Thus, for example, even with Select/Check/Operate systems the operator can cancel points or re-select new points. He can also perform other lower priority or non-control tasks such as selection of telemetry data while the highly secure functions are protected.

The EXECUTE PERMIT signal at Terminal J will be high when the EXECUTE A, B, C, and D commands are permitted to be sent; that is, the $\overline{\text{VERIFY}}$ = 0 and any aperture open conditions have been met. EXECUTE PERMIT may be used with a lamp driver card to illuminate the lamps inside the execute switches.

EXECUTE PERMIT

The actual three-bit command code which is sent to the remote is available at Terminals 14, 13, and 12. Table 1 is a truth table of the coding. It also shows the priority of the codes, with highest priority at the top.

COMMAND CODE

TABLE 1

COMMAND	LOGIC LEVELS AT TERMINALS		
	14	13	12
PT CANCEL	1	1	1
PT SELECT	1	1	0
EXECUTE A	1	0	1
EXECUTE B	1	0	0
EXECUTE C	0	1	1
EXECUTE D	0	1	0
EXECUTE E	0	0	1
EXECUTE F	0	0	0

The system normally requires a memory to store the address code of the point to be controlled. There are two terminals on the 66 CMDGEN available for loading the POINT MEMORY. Terminal 20 should be used in Select/Operate or Select/Check/Operate systems. It puts out a high level pulse each time the operator sends a PT SELECT command. Terminal 18 should be used in Direct Operate systems. It puts out a high-level pulse each time one of the four EXECUTE commands A, B, C, or D is sent.

SELECT POINT MEMORY LOAD

DIRECT OPERATE MEMORY LOAD

POINT MEMORY CLEAR

Terminal 22 is wired to the POINT MEMORY clear. It will pulse high for any PT CANCEL command or, if the Y1 Jumper is installed, when the aperture timer times out. If POINT MEMORY clear is not desired after the aperture closes, Jumper Y0 should be installed.

JUMPERS

RESET SELECTED POINT

Terminal 16 may be wired to the RESET SELECTED POINT input terminals of 66 LD/CD cards for systems in which it is desired to prevent an alarm at the selected point due to a change of state purposely caused by an EXECUTE A, B, C, or D command. This output will go to a logic 1 whenever one of the four EXECUTE commands is sent and the HALT RESET input at Terminal U is low. It will be reset by a PT SELECT or PT CANCEL command, by a high at HALT RESET or by the aperture time-out. This signal may be used for Select-type or Direct Operate systems.

HALT RESET

EXECUTE E LOAD

EXECUTE E LOAD is available at Terminal 21. It pulses high each time the EXECUTE E command is sent. Since the EXECUTE E and EXECUTE F commands are not involved with check back or aperture they may be used independent of the normal control commands EXECUTE A, B, C, or D. The EXECUTE E LOAD signal may be used, for example, to load selectable telemetry address codes into a memory.

APERTURE TIME JUMPER

APERTURE OPEN

The aperture timer has a variety of applications depending upon the system requirements. It does not have to be used, in which case the APERTURE TIME JUMPER is installed in the 0 position. If it is used, the APERTURE TIME JUMPER should be chosen for the number of seconds the aperture timer will be opened. As long as the aperture timer is opened, Terminal S will be high.

The aperture timer is opened and/or restarted each time a PT SELECT or an EXECUTE A, B, C, or D command is sent. At the end of its programmed period, it will close. A PT CANCEL command will close the timer immediately.

X JUMPERS

The 66 CMDGEN can be programmed to send a point cancel command automatically after the aperture times out. To do this, Jumper X1 must be installed, but, if that feature is not used, then JUMPER X0 should be installed.

RESET APERTURE

A high at Terminal T will reset the aperture and also cause the POINT MEMORY CLEAR, Terminal 22, to go high. This input is normally used in polled systems to inhibit undesirable control action when new remote stations are selected.

The 66 CMDGEN works together with the encoding controllers. The following connections should be made in the chassis wiring:

Signal Name	From 66 CMDGEN Terminal	To 66 ENC/L Terminal	
CIP	K	8 or J	CIP
DTLDD	W	17	DTLDD
LAGMI	N	4*	LAGMI

PWR ON PULSE

The card contains a power-failure detector. Terminal 19 will remain high as long as the input power drops below approximately 9 volts. The output will remain high for at least 19 mS after the power supply returns to a normal level. 2.5 seconds after Terminal 19 drops low, the unit will automatically send a PT CANCEL message.

2.5 SECOND DELAY

The 2.5-second delay timer is included on the board. It is guaranteed to last longer than the corresponding 2-second timer in the 66 CMDEC. All messages transmitted should be chosen such that the total number of bits sent divided by the baud rate is less than 1.6 seconds. The 2.5-second timer is started at the end of a power loss, when the aperture timer times out (if Jumper X1 is used), or from a MODE PULSE. When the 2.5 seconds is in progress, Terminal 17 will be high, and it may be used to blank various displays.

PULSE AFTER 2.5 SEC

The 2.5-second delay will end during Clock Ø4, and, at Ø7, Terminal M will pulse high. This signal may be used in the AUTO MODE to send the first message.

MANUAL MODE

Terminal P should be at a logic 1 when the ability of this card to send commands is desired, as in the MANUAL MODE. If the system does not have MODE, then Terminal P should be hard wired to a logic 1.

CLK OSC

CLK SYNC

Two clocking signals are brought off the board to drive and synchronize the clocking circuits on other cards as required to maintain the correct phase relationships. Terminal V is used to clock the input of an eight-stage counter, and Terminal 15 is tied to the reset line of the same counter. Refer to Figure 3 for connections and timing information.

*Also Terminals 7 and D of the 66 ENC/L should be jumped together.

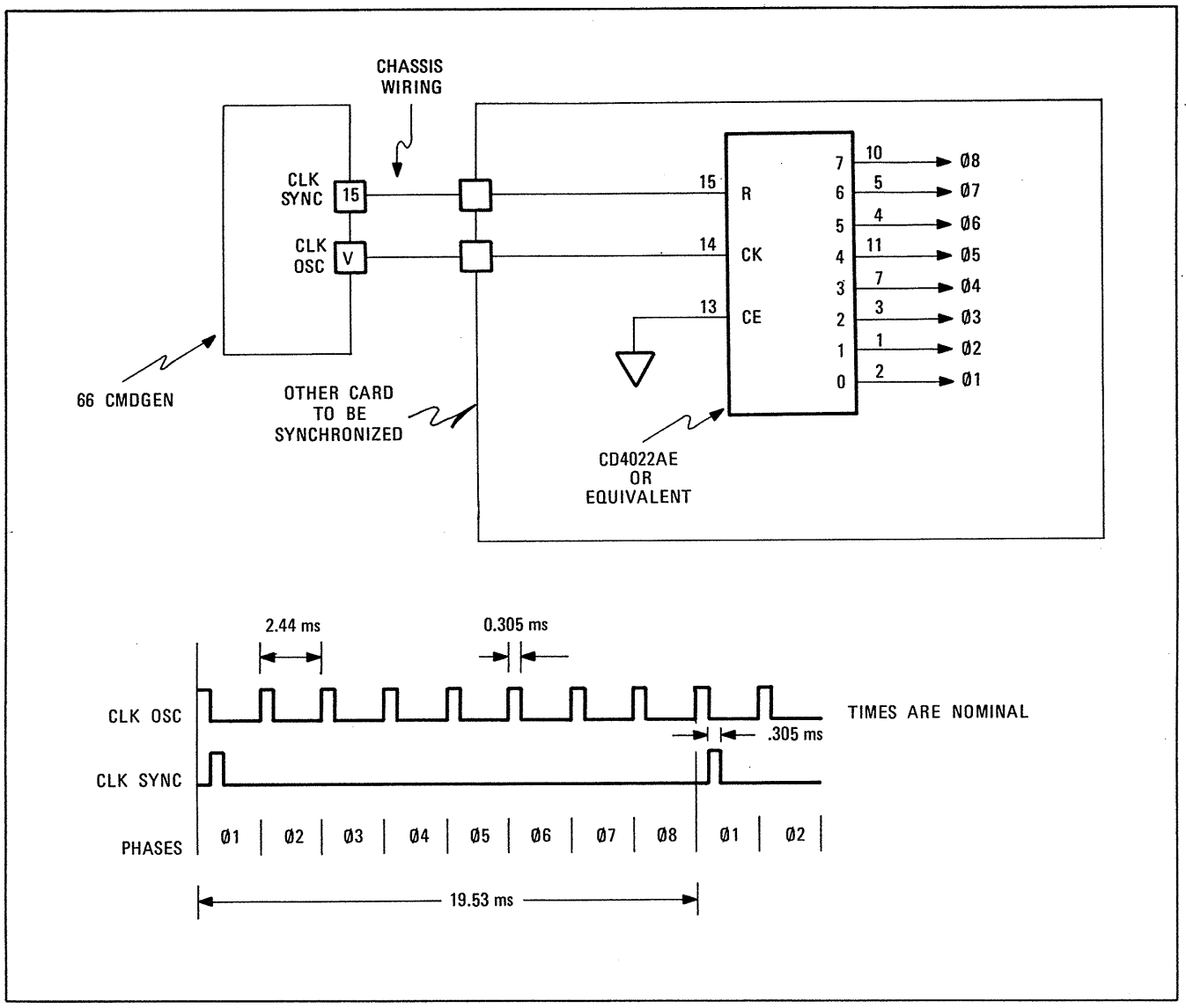

Figure 3. Method for clock synchronization, Model 66 CMDGEN.

THEORY OF OPERATION

The 66 CMDGEN utilizes multiphase clocking to assure that proper timing relationships exist both on the card and in the system. IC25, IC20A and associated resistors and capacitor (located at Zone A5 on Figure 4) form an oscillator, factory trimmed to 3276.8 Hz nominal. This frequency is divided by eight in IC24, (B4), and the eight phases are developed by IC23, (B5), even though only six are used. Figure 3 shows the timing relationship of the CLK OSC and CLK SYNC signals which are taken off the board to drive other modules.

If any of the command-input terminals on the left hand side of the schematic is raised to a logic 1, and assuming the gating requirements at IC3C, IC3D, IC4C, and IC4A (C2-3) have been met, then the output of IC2 (D5) will drop to a logic 0. The next time Ø6 occurs, a 0 will be clocked to IC7B-13, (E5). 19.5 mS later, at the next Ø6, a 1 will be clocked to IC7A-2, (E5), because its D input was 0. However, if the input signal had bounce and IC2-13 went high, even for an instant, IC7B would have been set, and the output of IC7A would have remained stable. Only if there has been no bounce for at least 19.5 mS continuously will IC7A-2 go high.

When IC7A-2 does go high, it clocks IC8B, (F5), which in turn clocks IC8A, IC22B (D4) and IC1 (D2). IC8A, in conjunction with IC15C (G4), outputs a single pulse during Ø7 which is used to start the encoding process. When IC22B and IC1 are clocked, whatever information was available at their D inputs is transferred to their Q outputs, and it will remain there until the data has been loaded into the input shift registers associated with the encoding process. If IC22B had been set because of a PT CANCEL input, however, IC1 would have been immediately cleared.

The function of IC6 (D1) is to provide a binary address for the active input having the highest priority. Table 1 shows the codes in priority order, with PT CANCEL being the highest. Thus if two or more inputs are enabled at the same time, only the highest priority will be sent.

If ever the PT SELECT or EXECUTE E commands are to be sent, pulses will appear at Terminal 20 or 21 respectively. Terminal 18 is handled a little differently. The D input to IC22A (E2) will be high if ever an EXECUTE A, B, C, or D command is to be sent. It will go to a high at the start of Ø6. This information will be transferred to IC22A-1 and Terminal 18 approximately .92 mS later when IC24-7 goes high. This short delay is necessary for proper functioning of IC17B (E1) which will output a high from IC17B-12. IC17B will be reset by a PT SELECT command, by a high at Terminal U or an aperture closure.

A PT SELECT or an EXECUTE A, B, C, or D will open the aperture timer by causing IC5A-1 (E2) to go high. When this happens, IC18 (F2), IC11 (G2) and the flip-flop made of IC13D and IC14C (H2) will be reset. IC14C-10 will be high. When DTLDD at Terminal W goes high and resets IC1 (D2) and hence IC5A-1 drops low, IC18 can then count Ø3 pulses from IC15A (E1) and IC14A (E2). The output of IC13A (F2) will go high every 5 seconds and be counted and decoded by IC11 (G2). Depending upon which jumper is installed, sometime later IC17A-3 (G2) will go high and then so will IC17A-2. IC17A-2 will only be high for one clock phase, but it will set the IC13D/IC14C (H2) flip-flop and thus close the aperture. The time-out pulse can also be used to clear POINT MEMORY or to send a PT CANCEL command. When the aperture is closed, IC15A-1 (E2) will be low, and IC18 will not receive any more pulses to count.

If the 12 V input power ever drops below approximately 9 volts, no current will flow in R17 (E3) and there will be a 0 volt drop across it. Q1 (E3) will have no base drive, R19 will pull the collector down, and IC16C-6 (E3) will go high. This is also true during power-up until the power supply capacitors can be charged. When IC16C-6 is high, both IC21A and IC21B (F3) will be set and cause a logic 1 at Terminal 19.

After power returns to normal, a voltage drop will be developed across R17 sufficient to turn on Q1 and force IC16C-6 low. It will take two more Ø6, pulses until the output of IC21B-13 drops low.

IC13B and IC14B (G3) form a set-reset flip-flop. A pulse into IC14B will set the flip-flop, and IC14B-6 will drop low. IC9A-2 (F3) will also be low if the power is normal. IC9A-3 will be low, and IC19 (F3) can then count Ø4 pulses. After 2.5 seconds, IC19-13 (F3) will go high causing the flip-flop to reset and the output of IC14B will rise to a logic 1. This resets IC19 and also triggers IC10B (G4) until Ø8.

For 2.5 seconds IC13B-4 was high and kept IC7A (E5) and IC8B (F5) set. Hence IC8B-12 was 0. At Ø4, IC13B-4 dropped low and IC9B-4 (G4) went high because of IC10B (G4). Now at Ø6, with IC7B-13 (E5) equal to 0 and IC9D-11 (C4) equal to 1, a high is clocked into IC7A-2 which clocks a high to IC8B-12 and causes a PT CANCEL message to be sent.

When power is lost and IC21B-13 (F3) is high, the IC13B/IC14B (G3) flip-flop is held set and IC19 (F3) is held reset until the power returns to normal. It will then take 2.5 seconds as described above to automatically send a PT CANCEL message.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	RFL PART NO.
	Model 66 CMDGEN Command Generator (Assembly HB-44190)	
C1	Capacitor, tantalum, 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
C2	Capacitor, ceramic, 0.0022 μF, 10%, 100 V, Kemet CK12BX222K, or eq.	H-1007-1368
C3 - 10	Capacitor, ceramic, 470 pF, 10%, 100 V, Kemet CK12BX471K, or eq.	H-1007-1358
CR1	Diode, zener, 8.2 V, 5%, 400 mW, Type 1N756A	HA-37441
CR2	Diode, Type 1N914B	HA-26482
IC1	Hex, D-Type flip-flop, National 74C174N, or eq.	H-0615-52
IC2	8-input NOR gate, RCA CD4078BE, or eq.	H-0615-49
IC3, 15	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC4	Triple, 3-input AND gate, RCA CD4073BE, or eq.	H-0615-32
IC5	Dual, 4-input OR gate, RCA CD4072BE, or eq.	H-0615-42
IC6	8-Bit priority encoder, Motorola MC14532CP, or eq.	H-0615-53
IC7,8,10,17,21,22	Dual D-Type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC9, 12	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC11	Decade counter/divider, RCA CD4017AE, or eq.	H-0615-38
IC13	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC14	Triple, 3-input NOR gate, RCA CD4025AE, or eq.	H-0615-20
IC16	Hex inverter/buffer, RCA CD4049AE, or eq.	H-0615-7
IC18, 19	14-stage counter/divider, RCA CD4020AE, or eq.	H-0615-2
IC20	Hex buffer, non-inverting, RCA CD4050AE, or eq.	H-0615-11
IC23, 24	Divide-by-eight counter/divider, RCA CD4022AE, or eq.	H-0615-6
IC25	Operational amplifier, National LM301AN, or eq.	H-0620-76
Q1	Transistor, silicon, NPN Type 2N5087	HA-46143
R1 - 23	Resistor, fixed, composition, 5%, ¼W, value on schematic, Allen Bradley CB, or eq.	H-1009-(XXX)
R24	Resistor, metal-film, 121 K, 1%, 1/8 W, Type RN55D, per RFL Spec HA-38301	H-1510-1578
R25	Same as R24, value selected at factory for oscillator frequency of 3276.8 Hz	H-1510-(XXX)
–	Shorting bar	HA-42904
–	Schematic	HE-44194

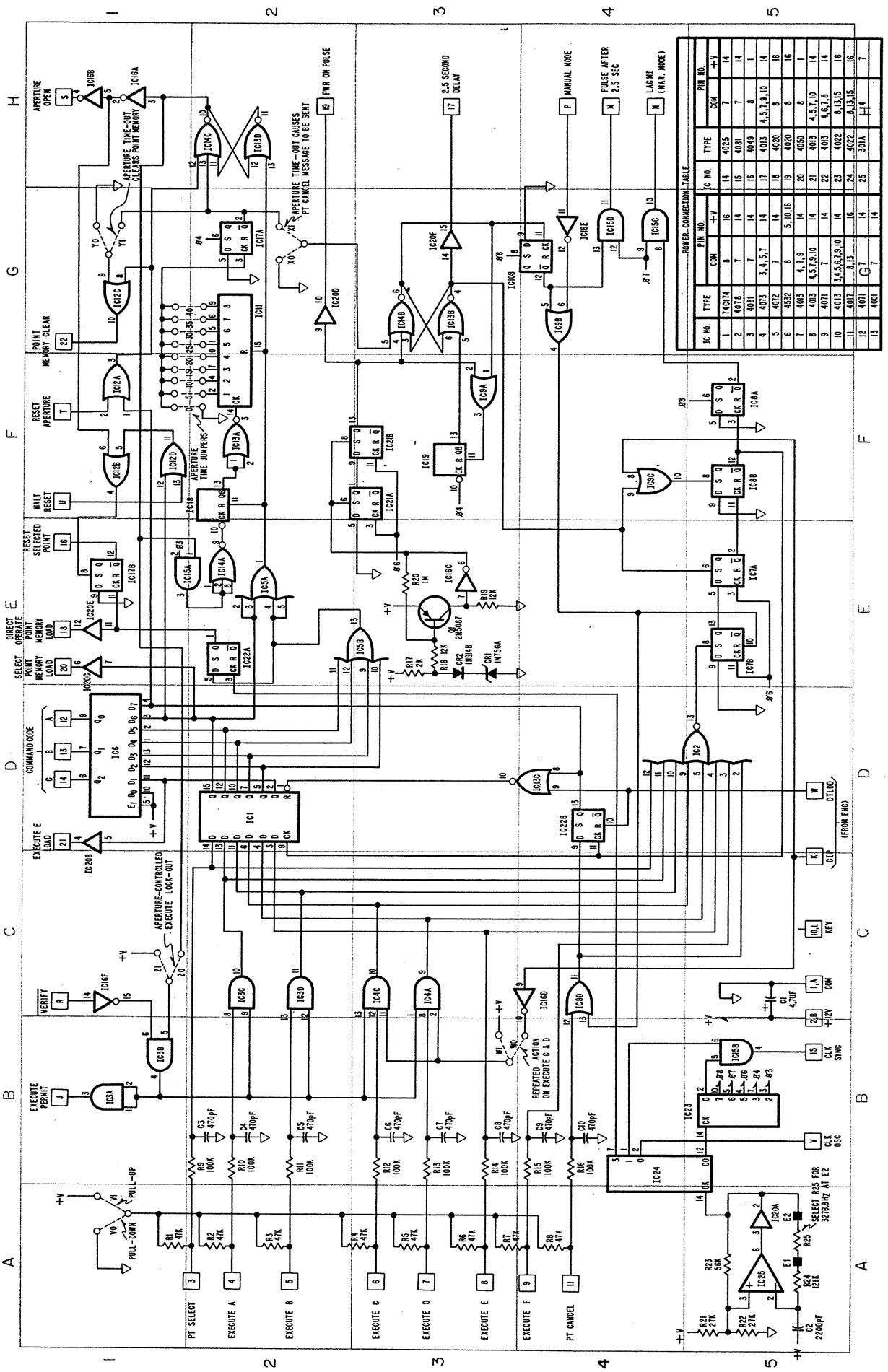

Figure 4. Schematic of Circuit, Model 66 CMDGEN.